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(54) Title: METHOD AND APPARATUS FOR CONTROLLING SIGNAL AMPLITUDE LEVEL <div style="text-align: center; margin-top: 20px;"> <pre> graph LR 20[Differential Input Signal] --> 22[VGA] 22 --> 24[Mean Square Calculator] 24 --> 26[Differential Operational Amplifier] 26 --> 26[Reference] 26 --> 26[Differential Output Signal] </pre> </div>		
(57) Abstract <p>An amplitude leveling circuit includes a variable gain, linear amplifier which receives an input signal and generates an output signal corresponding to the input signal. The signals may be in differential format. A signal processor receives the output signal and determines a corresponding mean squared signal. The signal processor includes a multiplier which squares the output signal, and an averager that averages the squared signal to generate the mean squared signal. An analyzer compares the mean squared signal with a reference and generates a feedback control signal that controls the gain of the variable gain amplifier in accordance with the difference between the mean squared signal and the reference value. The gain of the variable gain amplifier is controlled so that the amplitude of the output signal is maintained at a desired amplitude level without distorting the originally input waveform shape.</p>		

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**METHOD AND APPARATUS FOR
CONTROLLING SIGNAL AMPLITUDE LEVEL**

FIELD OF THE INVENTION

The present invention relates to amplitude leveling to ensure a signal's
5 amplitude maintains a constant level.

BACKGROUND OF THE INVENTION

In many signal processing applications, such as radio transceivers, it is
necessary to convert a signal with an unknown amplitude into a signal which has an
amplitude at a desired level. This amplitude control or "leveling," as it is sometimes
10 referred to hereafter, is performed for a variety of reasons including for example:

- to provide a constant drive level for frequency mixers for phase comparators
- to ensure that an amplifier input is not overdriven
- to remove unwanted amplitude noise from a signal.

15 Traditionally, amplitude leveling is performed using two different types of
circuits: limiters and automatic gain control (AGC) amplifiers with peak detection. As
will be explained below, each of these circuits suffers drawbacks.

Limiters provide a large signal gain and produce a constant output level
by "clipping," i.e., limiting, the signal peaks of input signals. Consequently, if a
20 sinusoidal type waveform is received at the input of the limiter, the limiting amplifier
produces a square wave output "clipping off" the positive and negative peaks of the
sinusoid. Limiter circuits are often employed in the back end of an FM receiver to
remove AM information from the received signal.

A significant drawback of limiters is their non-linearity. In the sinusoidal input example, the amplitude is effectively limited to a desired value but at great cost. The input sinusoidal waveform is distorted, and the output is more like a square wave than a sinusoid. Accordingly, limiter circuits are not appropriate in applications where
5 the linearity and waveform shape of the input signal must be preserved at the output. Examples of such applications include a receiver chain prior to out-of-band filtering, and a linear transmitter where harmonic levels must be controlled, or any signal processing performed on signals with amplitude modulation.

The other category of traditional amplitude levelers is AGC amplifiers
10 with peak detection. AGC amplifiers use feedback in an attempt to maintain signal wave shape as amplitude level is controlled. However, AGC amplifiers with peak detection detect either the negative or the positive peak of the signal rather than detecting the peak-to-peak level or the RMS level of the input signal. As a result, AGC levelers are not accurate for non-symmetrical signals.

15 There are other drawbacks with an AGC approach. AGC amplifiers with peak detection also do not operate on differential signals. This is a substantial problem for integrated circuit (IC) applications in which differential signals are commonly employed. Still further, AGC amplifiers with peak detection require a large capacitor to hold the peak value of the detected signal. Typically, such a capacitor is too large to be
20 integrated into solid state form, and therefore, it must be provided as a discrete component increasing the size and manufacturing costs of the amplitude limiting circuitry.

SUMMARY OF THE INVENTION

The present invention overcomes these problems in the prior art. Therefore, it is an object of the present invention to provide an amplitude leveling circuit and method which does not introduce distortion into the leveled signal.

5 It is an object of the present invention to provide an amplitude leveling circuit which does not require large, discrete components, such as large peak detector capacitors, and which is suitable for solid state integration.

 It is an object of the present invention to provide an amplitude leveling circuit that detects peak-to-peak or mean squared levels of input signals for accurate
10 amplitude leveling of non-symmetrical signals.

 It is a further object of the present invention to provide an amplitude leveling circuit that operates effectively on differential signals.

 The above-identified objects are met using an amplitude control circuit having a variable gain, linear amplifier which receives an input signal and generates an
15 output signal corresponding to the input signal. A signal processor receives the output signal and determines a corresponding mean squared signal. An analyzer compares the mean squared signal with a reference and generates a feedback control signal that controls the gain of the variable gain amplifier in accordance with the difference between the mean squared signal and the reference value. The gain of the variable gain
20 amplifier is controlled so that the amplitude of the output signal is maintained at a desired amplitude level without distorting the originally input waveform shape. To this end, the signal processor includes a multiplier which squares the output signal, and an averager that averages the squared signal to generate the mean squared signal.

In one preferred application, the amplitude control circuit is formed on an integrated circuit. Advantageously, the variable gain amplifier receives a differential input signal and generates a differential output signal. The differential output signal is squared and averaged, and a differential operational amplifier compares the averaged
5 signal with a reference. The resulting feedback signal controls the gain of the variable gain amplifier in accordance with the difference between the averaged signal and the reference value. In this way, the gain of the variable gain amplifier is controlled so that the amplitude of the differential output signal is maintained at a desired amplitude level while still preserving the waveform shape of the input signal.

10 In yet a more detailed, example embodiment, the amplitude control circuit includes a differential amplifier having a pair of differential signal input terminals connected to biasing terminals of a pair of transistors. A variable gain amplifier circuit receives differential signals produced by the differential amplifier and generates a differential output signal at a pair of differential signal output terminals. A multiplier
15 circuit squares the differential output signal. A current mirror connected to a reference current and to an output of the multiplier circuit generates a gain control signal connected to the variable gain amplifier.

A pair of DC level shifter circuits connect the pair of differential output terminals to the multiplier in order to generate differential output signals at two
20 different DC levels. The multiplier may be a Gilbert cell multiplier connected to a first current source, and a current source may be employed to generate the reference signal. The reference signal preferably has a predetermined relationship to the current generated by the first current source. In particular, the ratio of the currents generated by the first and second current sources is less than one. A capacitor is connected (among
25 other things) to the multiplier circuit output to low pass filter/average the squared differential output signal.

These features, objects, and advantages of the present invention will be described in further detail below in conjunction with the drawings and preferred, example embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

5 The present invention is illustrated by way of example and not limitation in the accompanying figures where like reference numerals indicate like elements and in which:

Fig. 1 shows an amplitude control circuit in accordance with one example embodiment of the present invention;

10 Fig. 2 shows another example embodiment of the present invention;

Fig. 3 is a flowchart diagram illustrating an example method in accordance with the present invention; and

Fig. 4 is another, more detailed embodiment of an amplitude control circuit in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

15 In the following description, for purposes of explanation and not limitation, specific details are set forth, such as particular embodiments, circuits, circuit components, etc. in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be
20 practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well-known methods, devices, and circuits are

omitted so as not to obscure the description of the present invention with unnecessary detail.

Fig. 1 illustrates a general example embodiment of an amplitude control circuit 10 in accordance with the present invention. An input signal is received at the input terminal of a linear variable gain amplifier (VGA) 12. The present invention has particularly advantageous application to analog input signals because the amplitude of the analog signal output from the linear variable gain amplifier 12 is limited to a desired level without distorting the waveform shape of the original input signal.

The variable gain amplifier output signal is processed in signal processor 14. In particular, the signal processor 14 determines a mean squared signal corresponding to the variable gain amplifier output signal. Squaring the signal permits accurate mean square detection of full waveforms, (rather than detection of only a positive or a negative peak), thereby providing accurate amplitude limiting for non-symmetrical signals. For purposes of this application the term "mean" includes authentic mean and average. The signal processor 14 may also determine a root mean squared (RMS) signal corresponding to the input if desired.

An analyzer 16 receives the mean squared output from signal processor 14 and compares it with a reference value. The output of analyzer 16 is fed back as a gain control signal to the linear, variable gain amplifier 12. The feedback control signal corresponds to a difference between the mean squared signal and the reference value and may be implemented as an integrating amplifier. The feedback control signal limits the output of the variable gain control amplifier 12 but without introducing distortion to the original input signal waveform. Moreover, signal amplitude in both positive and negative directions of the input waveform is detected to ensure that the output signal generated by variable gain amplifier is limited in RMS magnitude to a predetermined, desired level.

As mentioned above, a significant advantage of the present invention is that it does not require large components and may be formed on an integrated circuit. This advantage applies even more to a second example embodiment of an amplitude control circuit 20 in accordance with the present invention illustrated in Fig. 2.

5 In this second example solid state linear amplitude leveling circuit embodiment, the signals being processed are differential signals. The ability of the present invention to accurately process differential signals is a significant advantage over traditional, peak detection-based AGC level control circuits which lack this ability. Because differential signals are typically used in integrated circuits, the present
10 invention is particularly advantageous in controlling the amplitude level of integrated circuit signals.

 A linear, variable gain amplifier (VGA) 22 applies a variable gain in accordance with a feedback control gain signal to the differential input signal applied to positive (+) and negative (-) input terminals and generates a corresponding differential
15 output signal on positive and negative output terminals having a limited amplitude but without distorting the original waveform of the differential input signal. The differential output is processed by a mean squared calculator 24 which squares the differential output signal and then determines its average. A differential operational amplifier 26 compares the average signal generated by mean squared calculator 24 with
20 a reference signal to generate the feedback gain control signal for controlling the gain of the variable control amplifier 22.

 In both of the first and second example embodiments, the squaring function may be implemented using a multiplier, and a mean or an averaging function may be implemented using a low pass filter. Such a low pass filter typically uses only a
25 relatively small capacitor that can be readily integrated into an IC. In addition, while the reference value is typically constant when the desired amplitude level is to be

constant, the reference signal may also be a modulated value when the desired amplitude level changes. The output would then be a variable mean squared output.

Fig. 3 illustrates a set of procedures, referenced as amplitude control (block 30), for implementing an example of a method in accordance with the present invention. The input signal is received at a linear, variable gain amplifier and amplified in accordance with the currently set gain which can be greater or less than one (block 32). The output of the variable gain amplifier is then squared (block 34) and averaged (block 36). The averaged output signal is compared with a reference (block 38) to generate a feedback control signal corresponding to a difference between the average signal and the reference. The gain of the variable gain amplifier is controlled with the feedback control signal to ensure that the amplitude of the variable gain amplifier output signal is maintained at a desired amplitude level (block 40). As mentioned above, the amplitude of the output signal is maintained at the desired amplitude level without distorting the input signal. Moreover, the variable gain amplifier input and output signals may be differential signals.

Yet another example embodiment of the present invention is described in conjunction with the amplitude control circuit 50 illustrated in Fig. 4. The amplitude control circuit 50 includes a variable gain amplifier 52 connected to a pair of DC level shifters 54 and 56 which in turn are connected to a multiplier 58. The multiplier output is connected to an active load 60 which generates a gain control signal 62.

The variable gain amplifier includes six transistors Q_1 - Q_6 , resistors R_1 - R_4 , and power supplies V_{CC} and V_{bias} . A differential input (I/P) signal is received at the positive and negative terminals (the left-hand side) of the variable gain amplifier 52. The positive terminal is connected to the base of transistor Q_5 , and the negative terminal is connected to the base of transistor Q_6 . The amplifiers Q_5 and Q_6 form a differential pair, and resistors R_1 and R_2 are emitter degeneration resistors which

maintain a linear transconductance curve for transistors Q₅ and Q₆. As a result, the variable gain amplifier 52 is linear in operation.

Transistors Q₁-Q₄ perform a gain variation function. The collectors of transistors Q₅ and Q₆ are connected to the emitter coupled transistor pairs Q₁, Q₂, and Q₃, Q₄, respectively. A gain control signal 63 described in further detail below is connected to the base terminals of both transistors Q₁ and Q₄. The collectors of transistors Q₁-Q₄ are all connected to a standard DC voltage supplied at V_{CC}, and resistors R₃ and R₄ connected to the collectors of transistors Q₁ and Q₃ are load resistors. A biasing voltage V_{bias} is derived, for example, from V_{CC}. In effect, DC voltage is applied to the bases of transistors Q₂ and Q₃, and a variable (slowly-varying) voltage in the form of gain control signal 62 is applied to the bases of the other transistors Q₁ and Q₄ in the transistor pairs. In effect, transistors Q₁-Q₄ split a portion of the current from transistors Q₅ and Q₆. The current through transistors Q₁ and Q₄ is shunted to V_{CC}. The remaining portion of signal current through transistors Q₂ and Q₃ flows through resistors R₃ and R₄ thereby producing a signal voltage taken as the differential output signal.

The differential output signal terminals are also connected to two DC level shifters 54 and 56. These DC level shifters provide a fixed DC level shift, and at the same time, preserve AC waveform components of the output signal. The DC level shifters 54 and 56 are employed because transistors Q₇ through Q₁₀ require a first DC bias, and the transistors Q₁₁ and Q₁₂ require a second, lower DC bias. The output of the variable gain amplifier 52 is applied to both of these sets of transistors which is why each DC level shifter includes one input and two outputs.

One example way of implementing a DC level shifter is to use a series connected transistor resistor current source arrangement. Specifically, the bases of transistors Q₁₆ and Q₁₇ are connected to the output signal terminals at resistors R₃ and R₄. The emitter terminals of transistors Q₁₆ and Q₁₇ are used to drive the bases of

transistors Q7-Q10. After a voltage drop across respective emitter-connected resistors R5 and R6, a second lower voltage output signals from each of the DC level shifters 54 and 56 is connected to drive the base terminals of transistors Q12 and Q11, respectively,

The multiplier 58 is implemented as a well-known, Gilbert cell multiplier which includes transistors Q7-Q12 and resistors R7 and R8. Since Gilbert cell multipliers are conventional and well-known, no further description of the operation of the multiplier circuit 58 is believed necessary.

The outputs of the Gilbert cell multiplier 58 at collectors of transistors Q8 and Q10 are summed at node 62 in an active load 60. The active load 60 is a current mirror which includes transistors Q13 and Q14 connected at their base terminals. The current source I2 provides a reference current corresponding, for example, to the reference value shown as an input to differential operational amplifier 26 in Fig. 2. Preferably, current I2 is related to the current produced by current source I1 connected to the Gilbert multiplier 58 as shown in Fig. 4. The reference current I2 generates the current flowing through the transistor Q14. Since the transistors Q13 and Q14 are connected as a current mirror, the transistor Q13 attempts to reproduce that reference current I2 into the node 62.

In effect, the active load is comprised of both transistors Q13 and Q14. As a result, if the output current of transistors Q8 and Q10 is greater than the reference current in current source I2, then the voltage at node 62 decreases. If the output current of transistors Q8 and Q10 is less than the reference current generated by current source I2, then the voltage at node 62 increases.

Also connected to node 62 is a capacitor C1 connected to the common base of transistors Q13 and Q14. The capacitor C1 performs two functions: filtering the squared voltage present at node 62 and stabilizing the feedback loop function, i.e., the gain loop control signal 63. The filtering action of capacitor C1 performs a time

averaging of the squared signal. More specifically, higher frequency components of the voltage present at node 62 are attenuated by the capacitor so that the signal on the collector of transistor Q₁₃ is greatly attenuated for high frequencies. Assuming for example that the output signal of the variable gain amplifier 52 is a sine wave, the
5 squaring function implemented in multiplier 58 produces a DC level desired value for comparison to the reference signal. However, the squaring function also produces signal components at twice the frequency of the input signal and harmonics thereof. These higher frequency components are undesirable and are filtered out by the capacitor C₁. As mentioned above, the size of capacitor C₁ is relatively small and therefore may
10 be implemented in solid state form on an integrated circuit.

Because node 62 is a high impedance node and should not be loaded to other signal inputs without having a detrimental effect, an emitter-follower buffer, implemented as transistor Q₁₅, presents a high impedance to the collector of transistor Q₁₃. As a result of that high impedance, the signal level at the collector of transistor
15 Q₁₃ is not attenuated, and the current balance between transistors Q₈, Q₁₀, and Q₁₃ is preserved. Current source I₄ provides a biasing current for transistor Q₁₅ to keep that transistor active. The buffered signal from transistor Q₁₅ corresponding to gain control signal 63 controls the base voltage of transistors Q₁ and Q₄ which in turn modulates the gain of the variable gain amplifier 52.

20 Current source I₃ provides a bias current to ensure that transistors Q₁-Q₆ are all in an active state. Current source I₁ similarly provides a biasing current for the transistors in the multiplier circuit 58. In addition, current source I₁ maintains the relationship between currents I₁ and I₂ because the multiplier circuit output currents from transistors Q₈ and Q₁₀ is proportional to the bias current I₁. As a result, once the
25 feedback loop achieves steady state, the collector currents of transistors Q₈ and Q₁₀ are in a predetermined ratio of the current I₁. Therefore, I₂ is set to be a fraction of the current I₁. In general, the ratio of I₂ to I₁ will be between 0 and 1.

As described above, the present invention provides an amplitude control/leveling circuit and methodology that permits accurate leveling of asymmetric and differential signals using circuitry that can be readily implemented on an integrated circuit chip. Equivalent analog and digital circuitry may be employed to implement the functions described in conjunction with the above illustrative embodiments. The linear amplitude leveling control in accordance with the present invention does not introduce distortion and is suitable for solid state integration may be employed in any number of amplitude control environments, e.g., to level local oscillator signals used to drive a mixer, remove AC ripple, compensate for temperature variations, generate or detect AM modulation components, prevent amplifier overdrive, etc.

The invention has been described in terms of specific embodiments to facilitate understanding. The above embodiments, however, are illustrative rather than limitative. It will be apparent to one of ordinary skill in the art that departures may be made from the specific embodiments shown above without departing from the essential spirit and scope of the invention. Therefore, the invention should not be regarded as being limited to the above examples, but should be regarded instead as being fully commensurate in scope with the following claims.

WHAT IS CLAIMED IS:

1. An amplitude control circuit, comprising:
a variable gain amplifier receiving an input signal and generating an output
signal corresponding to the input signal;
5 a signal processor receiving the output signal and determining a corresponding
mean squared signal; and
an analyzer comparing the mean squared signal with a reference and generating a
feedback control signal connected to the variable gain amplifier for controlling the gain
of the variable gain amplifier in accordance with a difference between the mean squared
10 signal and the reference value,
wherein the gain of the variable gain amplifier is controlled so that the amplitude
of the output signal is maintained at a desired amplitude level.
2. The amplitude control circuit in claim 1, wherein the amplitude control
circuit is formed on an integrated circuit.
- 15 3. The amplitude control circuit in claim 1, wherein the signal processor
includes:
a multiplier squaring the output signal, and
an averager averaging the squared signal thereby generating the mean squared
signal.
- 20 4. The amplitude control circuit in claim 3, wherein the averager includes a
low pass filter.
5. The amplitude control circuit in claim 1, wherein the variable gain
amplifier is linear and the amplitude control circuit does not distort the input signal
waveform in generating the output signal.

6. The amplitude control circuit in claim 1, wherein the reference signal is a constant value associated with the desired amplitude level, and the desired amplitude level corresponds to a constant, mean squared output.

7. The amplitude control circuit in claim 1, wherein the reference signal is a modulated value associated with the desired amplitude level, and the desired amplitude level corresponds to a variable mean squared output.

8. The amplitude control circuit in claim 1, wherein the analyzer includes an operational amplifier.

9. An amplitude control circuit comprising:
10 a variable gain amplifier receiving a differential input signal and generating a differential output signal corresponding to the differential input signal;
a mean square calculator squaring the output differential signal and averaging the squared signal; and
a differential operational amplifier comparing the averaged signal with a
15 reference and generating a feedback control signal connected to the variable gain amplifier for controlling the gain of the variable gain amplifier in accordance with a difference between the averaged signal and the reference value,
wherein the gain of the variable gain amplifier is controlled so that the amplitude of the differential output signal is maintained at a desired amplitude level.

20 10. The amplitude control circuit in claim 9, wherein the variable gain amplifier is linear, and the amplitude control circuit does not distort the input signal waveform in generating the output.

11. The amplitude control circuit in claim 9, wherein the reference signal is a constant value associated with the desired amplitude level, and the desired amplitude
25 level corresponds to a constant, mean squared output.

12. A method, comprising the steps of:
receiving an input signal at a variable gain amplifier;
squaring an output of the variable gain amplifier;
averaging the squared output signal;
5 comparing the averaged output signal with a reference;
generating a feedback control signal corresponding to a difference between the
averaged signal and the reference; and
controlling the gain of the variable gain amplifier with the feedback control
signal so that the amplitude of the output signal is maintained at or below a desired
10 amplitude level.

13. The method in claim 12, wherein the squaring and averaging steps
correspond to generating a mean square of the output signal of the variable gain
amplifier.

14. The method in claim 12, the variable gain amplifier is linear, and the
15 method further comprising:
maintaining the amplitude of the output signal at the desired amplitude level
without distorting the input signal.

15. The method in claim 12, wherein the input signal and the output signal are
differentials signals.

20 16. An amplitude control circuit, comprising:
a differential amplifier having a pair of differential signal input terminals
connected to biasing terminals of a pair of connected transistors;
a variable gain amplifier circuit receiving differential signals produced by the
differential amplifier and generating a differential output signal at a pair of differential
25 signal output terminals;
a multiplier circuit for squaring the differential output signal; and

a current mirror connected to a reference current and to an output of the multiplier circuit for generating a gain control signal connected to the variable gain amplifier.

17. The amplitude control circuit in claim 16, further comprising:

5 a DC level shifter circuit connecting the pair of differential output terminals to the multiplier for generating the differential output signals at two different DC levels.

18. The amplitude control circuit in claim 16, wherein the multiplier is a Gilbert cell multiplier connected to a first current source.

19. The amplitude control circuit in claim 18, further comprising:

10 a second current source generating the reference signal,
wherein the reference signal is related to the current generated by the first current source.

20. The amplitude control circuit in claim 19, wherein the ratio of the currents generated by the second current source and the first current source is less than 1.

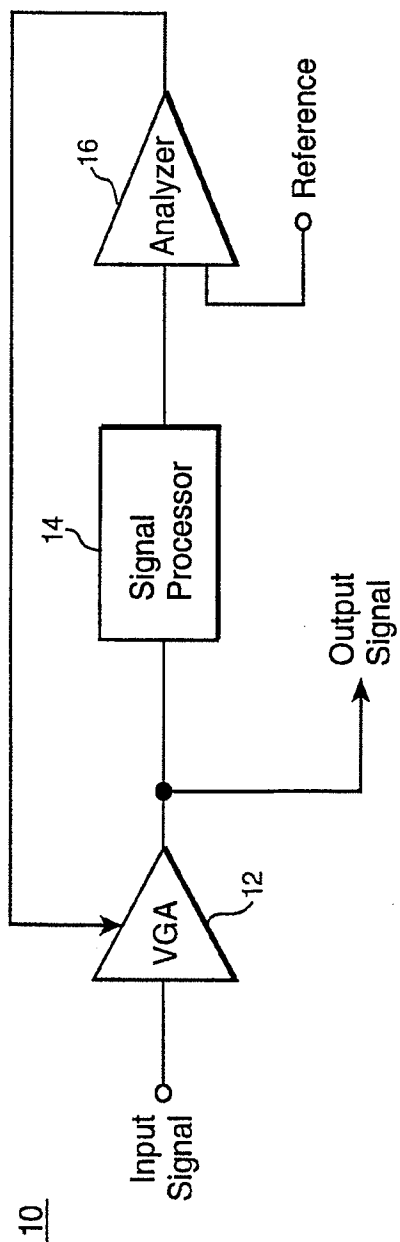
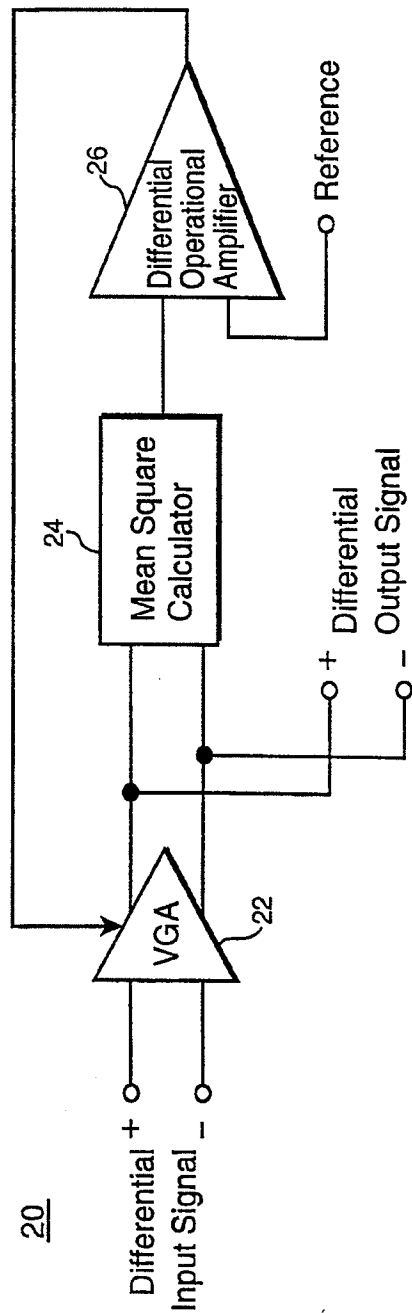
21. The amplitude control circuit in claim 16, further comprising:

15 a buffer amplifier connected between the current mirror output and the variable gain control circuit.

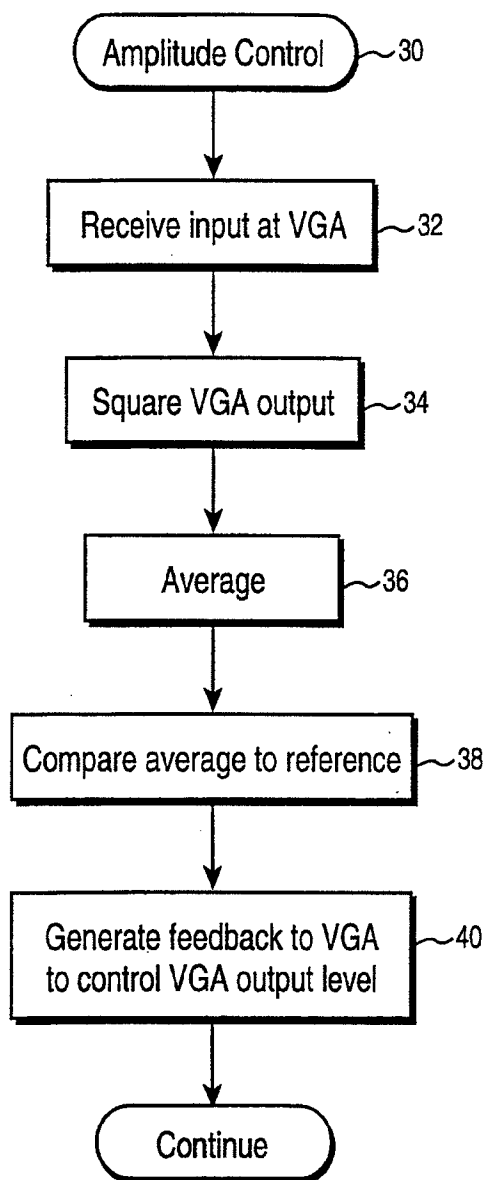
22. The amplitude control circuit in claim 16, wherein the variable gain amplifier is linear.

23. The amplitude control circuit in claim 16, further comprising:

20 a capacitor connected to the multiplier circuit, the current mirror, and the variable gain amplifier.

Fig. 1*Fig. 2*

2/3

*Fig. 3*

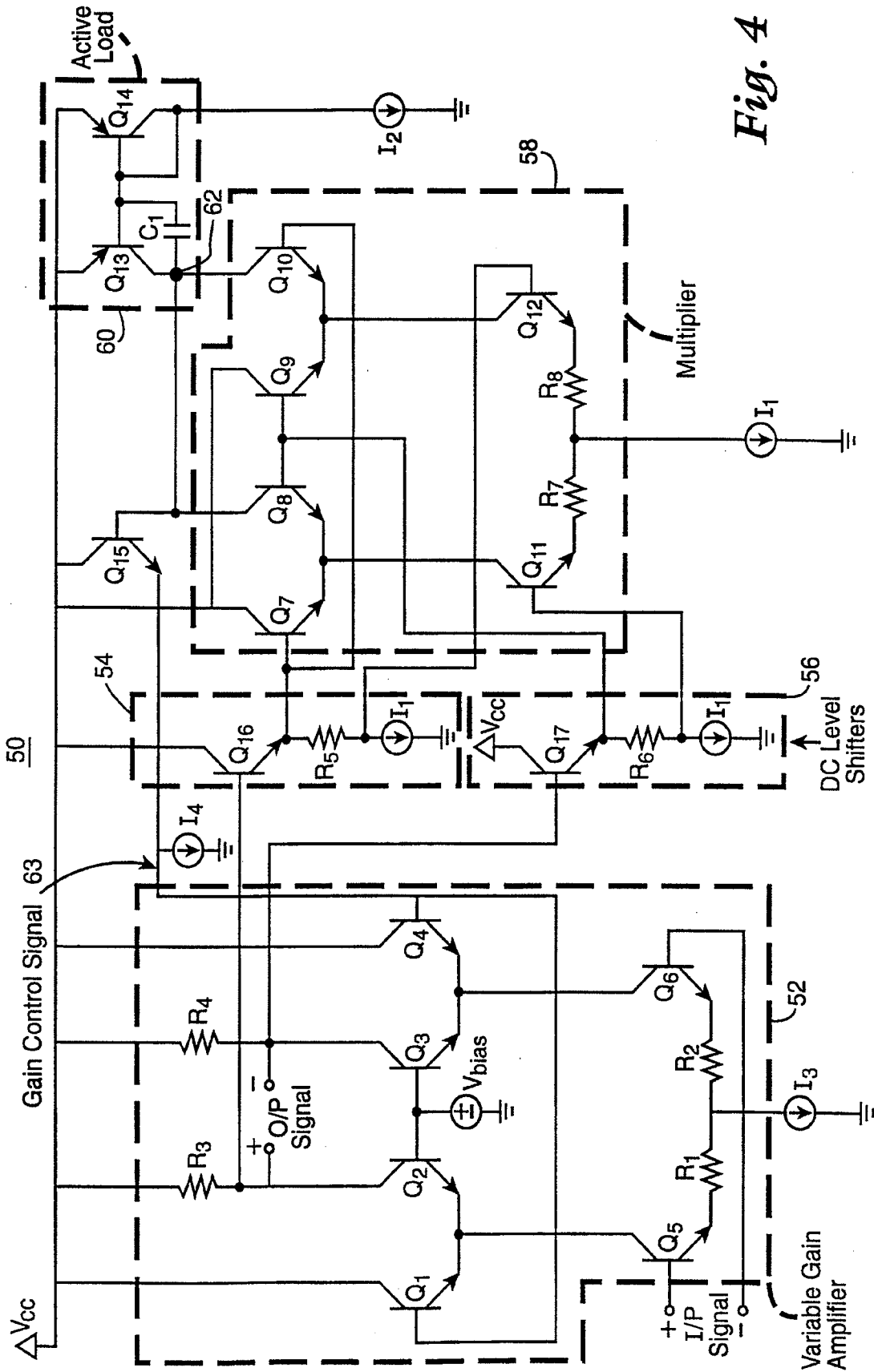


Fig. 4

INTERNATIONAL SEARCH REPORT

Int. Application No

PCT/US 98/14061

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03G3/30 H03G1/00

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H03G

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 546 050 A (BONEBRIGHT RODNEY K ET AL) 13 August 1996 see abstract see column 9, line 27 - column 10, line 33 see column 11, line 52 - column 12, line 8; figures 2,3,5,6 ---	1-4,9, 12,16
A	US 4 250 471 A (DUNCAN MICHAEL G) 10 February 1981 see abstract see column 4, line 40 - line 59; figure 2 ---	1,9,12, 16
A	US 5 642 075 A (BELL ANDREW G) 24 June 1997 see column 3, line 39 - column 5, line 5; figure 1 ---	1,9,12, 16
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

Int. Patent Application No

PCT/US 98/14061

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>HALONEN K ET AL: "INTEGRATED BICMOS IF-MODULES FOR MOBILE TELECOMMUNICATION APPLICATIONS" INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. (ISCAS), LINEAR CIRCUITS AND SYSTEMS (LCS), ANALOG SIGNAL PROCESSING (ASP) LONDON, MAY 30 - JUNE 2, 1994, vol. 5, 30 May 1994, pages 661-664, XP000592923 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS see abstract</p> <p style="text-align: center;">-----</p>	<p>1,9,12, 16</p>

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5546050 A	13-08-1996	NONE	
US 4250471 A	10-02-1981	NONE	
US 5642075 A	24-06-1997	NONE	